PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-188315
(43)Date of publication of application : 21.07.1998

(51)Int.Cl. G11B 7/125

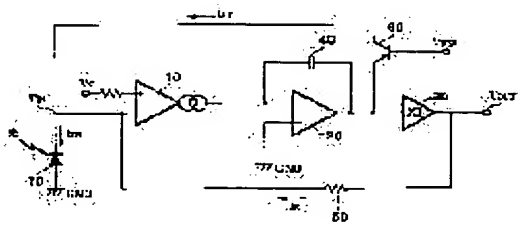
(21)Application number : 08-345086
(22)Date of filing : 25.12.1996

(71)Applicant : SONY CORP
(72)Inventor : SUZUKI ATSUSHI

(54) CURRENT/VOLTAGE TRANSFORMING CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a current/voltage transforming circuit by which a saturation state is avoided without reducing the trans-impedance and the S/N ratio is improved by providing a limiter in the circuit.

SOLUTION: A current IPH generated by a photodiode 70 in accordance with the incident light beam energy is transformed into voltage signals by amplifiers 10 and 20 and outputted through an output buffer 30. The emitter of a pnp transistor 60 is connected to the output terminal of the amplifier 20, the collector is connected to an input terminal TIN and a reference voltage VREF is applied to the base. When the current IPH is increased and the output voltage of the amplifier 20 exceeds (VREF+VBE), a limiter current ILT flow through the collector of the transistor 60 and limits a current IR which flows through a resistor element 50. Thus, the saturation state of the amplifiers 10 and 20 is prevented and the increase of the circuit delay time caused by the saturation is avoided.



LEGAL STATUS

[Date of request for examination] 11.06.2001
[Date of sending the examiner's decision of rejection]
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]